WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing
November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan
In conjunction with the 21st Asian Test Symposium (ATS'12)

Latest News!

Registration Desk and Hours
Hours:
November 22, 11:30~18:00
November 23, 8:30~16:00

Desk:
Entrance of Room 201B(2F) (See Guide Map Here)

Keynote Address (more detail: click the title!)
"Hardware Trojans: Threats and Emerging Solutions"
R. S. Chakraborty (Indian Institute of Technology, Kharagpur)

Invited Talk (more detail: click the title!)
"TRUDEVICE: a COST Action in Europe"
I. Polian (University of Passau)

"The Past and Future of WRTLT"
Y. Min (Chinese Academy of Sciences), H. Fujiwara (Osaka Gakuin University)

"System Level Testing Considerations as we Move from RTL to ESL"
Z. Navabi (University of Tehran)

Visa Guide information is now available!
WRTLT'12 Organizing Committee will send visa letters (confirmation letters) to attendees requesting them.
Please contact Registration Chair (e-mail: namba@ieee.org) if you request visa letters.

Related Links

- ATS'12
- PRDC'12

Information

SPONSORED BY

IEEE Computer Society Test Technology Technical Council

The IEICE Information and Systems Society,
Technical Committee on Dependable Computing

SCOPES

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'12, the thirteenth workshop, will be held in conjunction with the 21st Asian Test Symposium (ATS'12) in Niigata, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices and 3D ICs. Areas of interest include but are not limited to:

- High level Testing : RTL/Behavior level testing, High level approaches for testing, RTL ATPG, RTL DFT, RTL BIST, High level synthesis for testability, Relationship between RTL and gate level testing, Functional fault modeling,
- High level test bench generation
- 3D IC Testing
- SoC/Noc Testing: Test scheduling, Core testing, Interconnect testing
- Reliable SoC : System level reliability, Self repair, Fault tolerant SoC
- Microprocessor Testing
- Design Verification
- Gate Level Test Related Issues : Low power testing, Test compression, ATPG, DFT, BIST
- Secure Testing
- Hardware Trojan Detection

SUBMISSIONS

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. All submissions are now to be made electronically through the EasyChair conference system. Detailed instructions for submissions are to be found the website. Electronic submissions in PDF files are strongly recommended. Please visit the following website for submissions.

https://www.easychair.org/conferences/?conf=wrtlt12

Photocopies of accepted papers will be handed out to the attendees at the workshop site.

KEY DATES

- **Submission deadline: Sep. 9, 2012**
- Notification of acceptance: October 1, 2012
- Camera ready due: October 26, 2012

- Workshop days: November 22-23, 2012

WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing
November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan
In conjunction with the 21st Asian Test Symposium (ATS'12)

Latest News!

Registration Desk and Hours
Hours:
November 22, 11:30~18:00
November 23, 8:30~16:00

Desk:
Entrance of Room 201B(2F) (See Guide Map Here)

Keynote Address (more detail: click the title!)
"Hardware Trojans: Threats and Emerging Solutions"
R. S. Chakraborty (Indian Institute of Technology, Kharagpur)

Invited Talk (more detail: click the title!)
"TRUDEVICE: a COST Action in Europe"
I. Polian (University of Passau)

"The Past and Future of WRTLT"
Y. Min (Chinese Academy of Sciences), H. Fujiwara (Osaka Gakuin University)

"System Level Testing Considerations as we Move from RTL to ESL"
Z. Navabi (University of Tehran)

Visa Guide information is now available!
WRTLT'12 Organizing Committee will send visa letters (confirmation letters) to attendees requesting them.
Please contact Registration Chair (e-mail: namba@ieee.org) if you request visa letters.

Related Links

- ATS'12
- PRDC'12

Information

SPONSORED BY

IEEE Computer Society Test Technology Technical Council

The IEICE Information and Systems Society,
Technical Committee on Dependable Computing

SCOPES

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'12, the thirteenth workshop, will be held in conjunction with the 21st Asian Test Symposium (ATS'12) in Niigata, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices and 3D ICs. Areas of interest include but are not limited to:

- High level Testing : RTL/Behavior level testing, High level approaches for testing, RTL ATPG, RTL DFT, RTL BIST, High level synthesis for testability, Relationship between RTL and gate level testing, Functional fault modeling,
- High level test bench generation
- 3D IC Testing
- SoC/Noc Testing: Test scheduling, Core testing, Interconnect testing
- Reliable SoC : System level reliability, Self repair, Fault tolerant SoC
- Microprocessor Testing
- Design Verification
- Gate Level Test Related Issues : Low power testing, Test compression, ATPG, DFT, BIST
- Secure Testing
- Hardware Trojan Detection

SUBMISSIONS

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. All submissions are now to be made electronically through the EasyChair conference system. Detailed instructions for submissions are to be found the website. Electronic submissions in PDF files are strongly recommended. Please visit the following website for submissions.

https://www.easychair.org/conferences/?conf=wrtlt12

Photocopies of accepted papers will be handed out to the attendees at the workshop site.

KEY DATES

- **Submission deadline: Sep. 9, 2012**
- Notification of acceptance: October 1, 2012
- Camera ready due: October 26, 2012

- Workshop days: November 22-23, 2012

WRTLT'12 Advance Program

November 22, 2012

13:25 – 14:25
Plenary Session 1
Keynote Address
Hardware Trojan Detection at High Level
R. S. Chakraborty (Indian Institute of Technology, Kharagpur)
Invited Talk (1)
TRUDEVICE: a COST Action in Europe
I. Polian (University of Passau)

14:30 – 15:20
Session 1 High Level Testing & Secure Testing
1.1 Generating Directed Tests for C Programs using RTL ATPG
J. Raik, T. Drenkhan, M. Jenihhin, T. Viilukas, A. Karputkin, A. Chepurov R. Ubar (Tallinn University of Technology)
1.2 WAGSR: Web Application for Generalized Feed Forward Shift Registers (short)
K. Fujiwara (Akita University), H. Fujiwara (Osaka Gakuin University)
1.3 An Estimation of Trojan Circuits on AES Encryption Circuits (short)
M. Yoshimura (Kyushu University), A. Ogita, T. Hosokawa (Nihon University)

15:35 – 16:55
Session 2 Test Generation & Design for Testability
2.1 On detectability analysis of open faults using SAT-based test pattern generation considering adjacent lines
J. Yamashita, H. Yotsuyanagi, M. Hashizume (University of Tokushima), K. Kinoshita (Osaka Gakuin University)
2.2 Increasing Test Compaction Abilities of SAT-based ATPG through Fault Detection Constraints
S. Eggersglüß (DFKI), M. Diepenbeck, R. Wille (University of Bremen), R. Drechsler (DFKI)
2.3 Estimating the Number of Don't-Care Bits in Test Vectors
K. Miyase, S. Kajihara, X. Wen (Kyushu Institute of Technology)
2.4 A Test Point Insertion Method Using Don’t Care Identification and Test Compaction Techniques to Reduce Test Application Time for Transition Faults
T. Hosokawa, A. Takahashi, H. Yamazaki (Nihon University), M. Yoshimura (Kyushu University)

17:00 – 18:15

Session 3 Reliability & Dependable SoC

3.1 Which Metric is Better for Quantification of Hardware Faults-induced Errors?
Y. Fang, H. Li, X. Li (Chinese Academy of Sciences)
3.2 A Realization Method of Fast and Dependable Programmable Logic Controllers
R. Kawaguchi, Y. Yamada, K. Takahashi, Y. Urano, Y. Iguchi (Meiji University)
3.3 An Efficient Fault Simulation Algorithm for Analyzing Incorrect State Transitions Induced by Soft Errors in Sequential Circuits
T. Takata, M. Yoshimura, Y. Matsunaga (Kyushu University)
3.4 A Study on Error Correctable Test Pattern Generator for Reliable Built-in Self Test (short)
Y. Fukazawa, T. Iwagaki, H. Ichihara, T. Inoue (Hiroshima City University)

November 23, 2012

9:00 – 10:10

Plenary Session 2

Invited Talk (2)

The Past and Future of WRTLT
Y. Min (Chinese Academy of Sciences), H. Fujiwara (Osaka Gakuin University)

Invited Talk (3)

System Level Testing Considerations as we Move from RTL to ESL
Zainalabedin Navabi (University of Tehran)

10:25 – 11:40

Session 4 Delay Testing

4.1 Capturing Post-Silicon Variations by Layout-Aware Path-Delay Testing
X. Zhang, J. Ye, Y. Hu, X. Li (Chinese Academy of Science)
4.2 Exact and Heuristic Methods of Generating Compact Tests for Hold-time Violations
T. Iwagaki, H. Ichihara, T. Inoue (Hiroshima City University), K. K. Saluja (University of Wisconsin-Madison)
4.3 A Reduction Technique of Volume of Input Sequences for Time-Multiplexed Delay Measurement Using Embedded Delay Measurement Circuit
K. Katoh, S. Hoshina Tsuruoka (Tsuruoka National College of Technology), K. Itagaki (Nagaoka University of Technology)
4.4 Delay measurement of global routing resources in FPGA for small delay defect detection (short)
Kazuteru Namba, Nobuhide Takashina, Hideo Ito (Chiba University)

13:10 – 14:20
Panel Session

Theme: "Can RTL test techniques be applied to software?"
Coordinator: J. Raik (Tallinn University of Technology)
Panelists:
Dr. Görschwin Fey, Bremen University/ German Institute for Aerospace DLR, Germany
Prof. Masahiro Fujita, University of Tokyo, Japan
Prof. Zainalabedin Navabi, University of Tehran, Iran/ Worcester Polytechnic Institute, US
Prof. Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, China

14:25 – 15:40
Session 5 Low Power Testing & Random Testing & Online Testing

5.1 Analysis on the Effect of Distance Hypothesis in Anti-Random Testing
S. Gu, S. Xu, Y. Wu (Shanghai University)
5.2 Power Aware Scan Flip Flop Design for Scan Test
S. Ahlawat (Indian Institute of Technology, Bombay), A. K. Suhag (Gautam Buddha University), J. T. Tudu (Indian Institute of Science, Bangalore), V. Singh (Indian Institute of Technology, Bombay)
5.3 An Improved Method of Per-Cell Dynamic IR-Drop Estimation Based on the Weighted Switching Activity Metric
Y. Yamato, Y. Akiyoshi, T. Yoneda, K. Hatayama, M. Inoue (NAIST)
5.4 An Online Method for Serial Interconnects Testing (short)
S. S.-Kohan, S. Keshavarz, Z. Navabi (University of Tehran)

16:10 – 17:15
Session 6 SoC/NoC Testing & 3D IC Testing

6.1 Output Voltage Estimation Method of Hard Open TSV in 3D ICs
M. Hashizume, S. Kondo, E. Haraguchi, H. Yotsuyanagi (University of Tokushima), T. Tada (Tokushima Bunri University), Z. Roth (Florida Atlantic University)
6.2 A Cost-Effective Scheme for 3-D Stacked NoC Router and Interconnect Testing (short)
D. Xiang (Tsinghua University)
6.3 On Automating The IEEE 1500 Core Wrapper Insertion for SOC Testing (short)
M. I. M. Ibrahim, F. A. Hussin (Universiti Teknologi PETRONAS)
6.4 An Algorithm for Core-Based Test Time Optimization for 3-D Integrated Circuits (short)
M. Pradhan (Jadavpur University), C. Giri, H. Rahaman (Bengal Engineering and Science University, Shibpur) , D. K. Das (Jadavpur University)

WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing
November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan
In conjunction with the 21st Asian Test Symposium (ATS'12)

Visa Guide

WRTLT'12 Organizing Committee will send visa letters (confirmation letters) to attendees requesting them. Please contact Registration Chair (e-mail: namba@ieee.org) if you request visa letters.

WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing
November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan
In conjunction with the 21st Asian Test Symposium (ATS'12)

Accommodation

Collocated conferences PRDC2012 and ATS2012 differently offer the rooms in the following hotels at the discount rates. Please use the registration links of the conference websites **PRDC2012** and **ATS2012**. Note that even for the same hotel, room rates offered by PRDC and the ones by ATS are unfortunately different.

PRDC2012 (Conference rates are valid for the stay from 17 Nov. to 23 Nov.)

- Hotel Okura Niigata
- Hotel Nikko Niigata
- ANA Crowne Plaza Hotel Niigata
- Niigata Tokyu Inn

ATS2012 (Conference rates are valid for the stay from 18 Nov. to 23 Nov.)

- Hotel Nikko Niigata
- ANA Crowne Plaza Hotel Niigata
- Niigata Tokyu Inn
- Niigata Daiichi Hotel
- Niigata Station Hotel

General Chair
M. Hashizume, U Tokushima, Japan

General Vice-Chair
M. Inoue, NAIST, Japan

Program Chair
T. Hosokawa, Nihon U, Japan

Panel Chair
X. Wen, Kyutech, Japan

Finance Chair
M. Yoshimura. Kyushu U, Japan

Publicity Chair
K. Miyase, Kyutech, Japan

Publications Chair
T. Asakawa, Tokai U, Japan

Registration Chair
K. Namba, Chiba U, Japan

Local Arrangements Chair
S. Fukumoto, TMU, Japan

Audio Visual Chair
T. Iwagaki, Hiroshima City U, Japan

Ex Officio
K. Hatayama, NAIST, Japan

Program Committee

M. Arai, TMU, Japan
R. S. Chakraborty, IIT, Kharagpur, India
J. Dworak, Southern Methodist University, USA
M. -L. Flottes, LIRMM, France
H. Ichihara, Hiroshima City U, Japan
S. Kajihara, Kyutech, Japan
M. A. Kochte, U Stuttgart, Germany
E. Larsson, Lund U, Sweden
C. -M. Li, National Taiwan U, Taiwan
H. Li, Chinese Academy of Sciences, China
S. Ohtake, Oita U, Japan
I. Polian, U Passau, Germany
J. Raik, Tallinn U, Estonia
M. S. Reorda, Politecnico di Torino, Italy
S. Safari, U Tehran, Iran
V. Singh, IIT Bombay, India
N. Touba, U Texas, USA
D. Xiang, Tsinghua U, China
T. Yoneda, NAIST, Japan
H. Yotsuyanagi, U Tokushima, Japan

Final CALL FOR PAPERS

WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing

November 22-23, 2012, Toki Messe, Niigata, JAPAN

In conjunction with the 20th Asian Test Symposium (ATS'12) in Niigata

Sponsored by

IEEE Computer Society Test Technology Technical Council

Technical Committee on Dependable Computing, Information and Systems Society, the IEICE

SCOPE

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'12, the 13th workshop, will be held in conjunction with the 21th Asian Test Symposium (ATS'12) in Niigata, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices and 3D ICs. Areas of interest include but are not limited to:

- High level Testing : RTL/Behavior level testing, High level approaches for testing, RTL ATPG, RTL DFT, RTL BIST, High level synthesis for testability, Relationship between RTL and gate level testing, Functional fault modeling,
- High level test bench generation
- 3D IC Testing
- SoC/Noc Testing: Test scheduling, Core testing, Interconnect testing
- Reliable SoC : System level reliability, Self repair, Fault tolerant SoC
- Microprocessor Testing
- Design Verification
- Gate Level Test Related Issues : Low power testing, Test compression, ATPG, DFT, BIST
- Secure Testing
- Hardware Trojan Detection

SUBMISSIONS

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. Good papers will be offered to be submitted to the journal of the Institute of Electronics, Information and Communication Engineers (IEICE). All submissions are now to be made electronically through the EasyChair conference system. Detailed instructions for submissions are to be found the website. Electronic submissions in PDF files are strongly recommended. Please visit the following website for submissions.
https://www.easychair.org/conferences/?conf=wrtlt12

KEY DATES

Submission deadline: Sep. 9, 2012
Notification of acceptance: September 28, 2012
Camera ready due: October 26, 2012

Photocopies of accepted papers will be handed out to the attendees at the workshop site.

FURTHER INFORMATION

WWW: http://www.ieee-wrtlt.org/2012/ E-mail: wrtlt12@aries30.cse.kyutech.ac.jp

WRTLT Steering Committee
Tomoo Inoue (Hiroshima City University, Japan) Chair
Dong Xiang (Tsinghua University, China) Vice-Chair
Masaki Hashizume (The University of Tokushima, Japan)
Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan)
Xiaowei Li (Chinese Academy of Sciences, China)
Kewal K. Saluja (University of Wisconsin, USA)
Hideo Fujiwara (Osaka Gakuin University, Japan)
Hideo Tamamoto (Akita University, Japan)
Toshinori Hosokawa (Nihon University, Japan)
Erik Larsson (Linkoping University, Sweden)
Alex Orailoglu (University of California, San Diego, USA)
Virendra Singh (Indian Institute of Science, India)
Dafang Zhang (Hunan University, China)

WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing
November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan
In conjunction with the 21st Asian Test Symposium (ATS'12)

Information
- Scopes
- Submissions
- Key Dates

Registration
- Registration

WRTLT'12 Program
- Advance Program

Visa Guide
- Visa Guide

Accommodation
- Accommodation

Location
- The Venue

Call for Papers
- PDF

Committees
- Organizing Committee
- Program Committee
- Steering Committee

Related Links
- ATS'12
- PRDC'12

Committees

Organizing Committee

- General Chair
  Masaki Hashizume, University of Tokushima, Japan
- General Vice-Chair
  Michiko Inoue, Nara Institute of Science and Technology, Japan
- Program Chair
  Toshinori Hosokawa, Nihon University, Japan
- Panel Chair
  Xiaoqing Wen, Kyushu Institute of Technology, Japan
- Finance Chair
  Masayoshi Yoshimura, Kyushu University, Japan
- Publicity Chair
  Kohei Miyase, Kyushu Institute of Technology, Japan
- Publications Chair
  Takeshi Asakawa, Tokai University, Japan
- Registration Chair
  Kazuteru Namba, Chiba University, Japan
- Local Arrangements Chair
  Satoshi Fukumoto, Tokyo Metropolitan University, Japan
- Audio Visual Chair
  Tsuyoshi Iwagaki, Hiroshima City University, Japan
- Ex Officio
  Kazumi Hatayama, Nara Institute of Science and Technology, Japan

Program Committee

- Masayuki Arai, Tokyo Metropolitan University, Japan
- Rajat Subhra Chakraborty, Indian Institute of Technology, India
- Jennifer Dworak, Southern Methodist University, USA
- Marie-Lise Flottes, LIRMM, France
- Hideyuki Ichihara, Hiroshima City University, Japan
- Seiji Kajihara, Kyushu Institute of Technology, Japan
- Michael A. Kochte, University of Stuttgart, Germany
- Erik Larsson, Lund University, Sweden

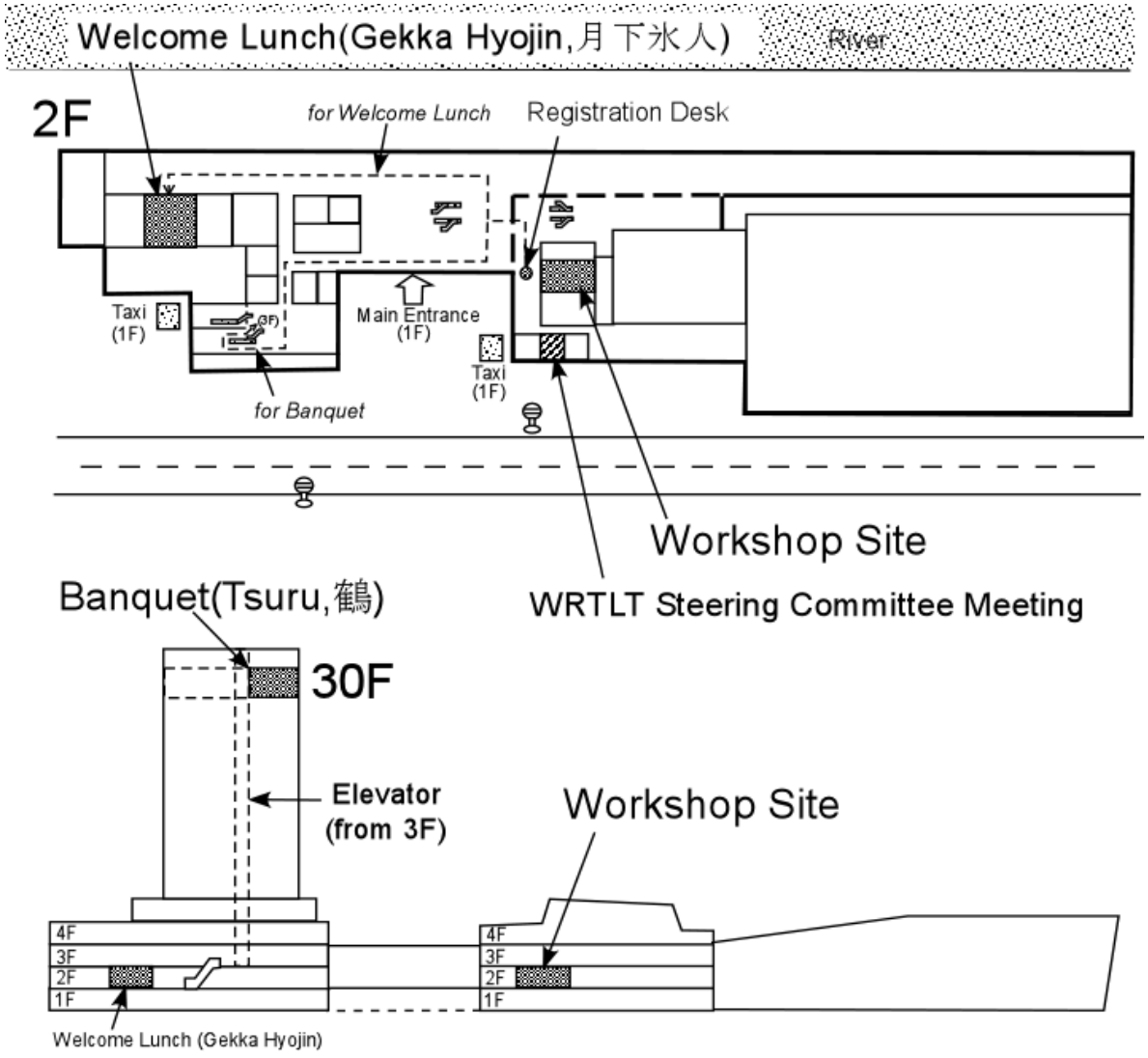
- Chien-Mo Li, National Taiwan University, Taiwan
- Huawei Li, Chinese Academy of Sciences, China
- Satoshi Ohtake, Oita University, Japan
- Ilia Polian, University of Passau, Germany
- Jaan Raik, Tallinn University of Technology, Estonia
- Matteo Sonza Reorda, Politecnico di Torino, Italy
- Saeed Safari, University of Tehran, Iran
- Virendra Singh, IIT Bombay, India
- Nur Touba, University of Texas, USA
- Dong Xiang, Tsinghua University, China
- Tomokazu Yoneda, Nara Institute of Science and Technology, Japan
- Hiroyuki Yotsuyanagi, University of Tokushima, Japan

Steering Committee

- Chair: Tomoo Inoue, Hiroshima City University, Japan
- Vice-Chair: Dong Xiang, Tsinghua University, China
- Hideo Fujiwara, Osaka Gakuin University, Japan
- Masaki Hashizume, The University of Tokushima, Japan
- Toshinori Hosokawa, Nihon University, Japan
- Kazuhiko Iwasaki, Tokyo Metropolitan University, Japan
- Erik Larsson, Linkoping University, Sweden
- Xiaowei Li, Chinese Academy of Sciences, China
- Alex Orailoglu, University of California, San Diego, USA
- Kewal K. Saluja, University of Wisconsin, USA
- Virendra Singh, Indian Institute of Science, India
- Hideo Tamamoto, Akita University, Japan
- Dafang Zhang, Hunan University, China

WRTLT' 12 Accommodation

- *Workshop:* Room 201B(2F)
  Nov. 22, 13:25 – 18:05, Nov. 23, 9:00 – 17:00
- *Welcome Lunch:* Gekka Hyojin(月下氷人)(2F)
  Nov. 22, 12:00 – 13:15
  (You will be served a lunch box at the lunch time in Nov. 23.)
- *Banquet:* Tsuru(鶴), Hotel Nikko Niigata(30F)
  Nov. 22, 18:30 – 20:30
- *WRTLT Steering Committee Meeting:* Room 203(2F)
  Nov. 23, 11:40 – 13:00



WRTLT'12

The Thirteenth Workshop on RTL and High Level Testing
November 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan
In conjunction with the 21st Asian Test Symposium (ATS'12)

Information
- Scopes
- Submissions
- Key Dates

Registration
- Registration

WRTLT'12 Program
- Advance Program

Visa Guide
- Visa Guide

Accommodation
- Accommodation

Location
- The Venue

Call for Papers
- PDF

Committees
- Organizing Committee
- Program Committee
- Steering Committee

Related Links
- ATS'12
- PRDC'12

Keynote Adress & Invited Talks

Keynote Adress

"Hardware Trojans: Threats and Emerging Solutions"

(Plenary Session 1; 13:25-14:25, Nov. 22, 2012)

Rajat Subhra Chakraborty
(Indian Institute of Technology, Kharagpur)

Summary: Economic reasons dictate the widespread participation of external agents in modern design and manufacture of integrated circuits (ICs), which decreases the control that the IC design houses used to traditionally have over their own designs. In this scenario, malicious, hard-to-detect circuit modifications made during the design or manufacturing steps, commonly known as "hardware Trojans" have emerged as a major security concern. This issue raises the question of ensuring Trust in an integrated circuit, and whether the entire design and manufacturing flow can be certified to be secure. A satisfactory answer to this question is of paramount importance in gaining trust about the result of the information processing carried out by the systems of which the ICs are a part. In this tutorial, we would explore the threat posed by Hardware Trojans, and testing techniques to detect them.

Biography: Dr. Rajat Subhra Chakraborty is an Assistant Professor in the Computer Science and Engineering Department of IIT Kharagpur, India. He has a Ph.D. in Computer Engineering from Case Western Reserve University, USA. His professional experience includes a stint as CAD Software Engineer at National Semiconductor (India Design Centre), and a graduate internship at Advanced Micro Devices (AMD).

His primary research interest is hardware security, including design methodology for hardware IP/IC protection, hardware Trojan detection/prevention through design and testing, attacks on hardware implementation of cryptographic algorithms, and reversible watermarking for digital content protection. He has close to 40 publications in international journals and conferences of repute. He has delivered tutorials at several international conferences and workshops, and has rendered his service as a reviewer and program committee member for multiple international conferences and journals. He is the co-author of one book on hardware security (forthcoming). He is a recipient of the "IBM Faculty Award" for 2012. Two patents have been filed based on his research work. Dr. Chakraborty is a member of IEEE.

Invited Talks

"TRUDEVICE: a COST Action in Europe"

(Plenary Session 1; 13:25-14:25, Nov. 22, 2012)

Ilia Polian (University of Passau)

Summary: Hardware security is becoming increasingly important for many embedded systems applications ranging from small RFID tag to satellites orbiting the earth. Its relevance is expected to increase in the upcoming decades as secure applications such as public services, communication, control and healthcare will keep growing. The vulnerability of hardware devices that implement cryptography functions (including smart cards) has become the Achille's heel in the last decade. Therefore, the industry is recognizing the significance of hardware security to combat semiconductor device counterfeiting, theft of service and tampering.
The recently approved COST Action "Trustworthy Manufacturing and Utilization of Secure Devices" aims at creating a European network of competence and experts on all aspects of hardware security including design, manufacturing, testing, reliability, validation and utilization. The network will play a key role in developing solutions responding to the hardware security challenges.

Biography: Ilia Polian is a Full Professor of Computer Engineering and the Vice Dean of Faculty of Informatics and Mathematics at the University of Passau, Germany. He received his PhD degree in 2003 from the University of Freiburg, Germany. His research interests include test methods, robustness, security, and quantum circuits. He is IEEE Senior member, has over 100 publications, won one best paper award and one best paper award nomination. He was involved in organization of several conferences, including IEEE European Test Symposium 2007 in Freiburg and Test Methods and Reliability workshop 2011 in Passau. He is Vice Chair of the German (GI/VDE/VDI) focus group on Test Methods and Reliability.

"The Past and Future of WRTLT"

(Plenary Session 2; 9:00-10:10, Nov. 23, 2012)

Yinghua Min (Chinese Academy of Sciences)

Hideo Fujiwara (Osaka Gakuin University)

Summary: The paper recalls the establishment, and development of the IEEE workshop on RTL and High Level Testing. This workshop has run for 12 years, and has brought researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences inregister transfer level (RTL) and high level testing. However, since nano-scale ICs are confronting material and fabrication technology challenges, it might be hard for computer scientists to provide new ideas on this kind of ICs testing. In addition, many people pay attention to paper publication, which is not a major issue for aworkshop. In order to re-activate the workshop, authors suggest some ideas for consideration.

Biography: YINGHUA MIN graduated from Mathematics Department of Jilin University in1962, and completed his post-graduate study at China Academy of Railway Sciences in 1966. He has visited Stanford and other universities in the US for years since 1981. He is now an emeritus professor of Computer science at Institute of Computing Technology, Chinese Academy of Sciences, the honorary Chair of technical committee on fault-tolerant computing, China Computer Federation. He published 250 technical papers, and 4 books, and received the Natural Science awards three times from the Chinese Academy of Sciences. He served on the editorial board of Journal of Electronics Testing, and as the Executive Editor-in-Chief of Journal of Computer Science and Technology. He was a member of IEEE CS Fellow Committee and numerous program committees of IEEE international conferences, the general co-chair of IEEE ATS'98 in Singapore and IEEE PRDC'99 in Hong Kong, and was the steering committee chair of IEEE WRTLT and received the meritorious service award from IEEE Computer Society in 2001. His current research interests include electronic testing, dependable computing, software reliability, and networking. He is a Fellow of IEEE, and a golden core member of IEEE CS.

Biography: HIDEO FUJIWARA received the B.E., M.E., and Ph.D. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1969, 1971, and 1974, respectively. He was with Osaka University from 1974 to 1985, Meiji University from 1985 to 1993, Nara Institute of Science and Technology (NAIST) from 1993 to 2011, and joined Osaka Gakuin University in 2011. Presently he is Professor Emeritus of NAIST and a Professor at the Faculty of Informatics, Osaka Gakuin University, Osaka, Japan. He has published over 400 papers in refereed journals and conferences, and nine books including the book from the MIT Press (1985) entitled “Logic Testing and Design for Testability.” He received several awards such as IEEE Computer Society Meritorious Service Awards in 1996 and 2005, IEEE Computer Society Continuing Service Award in 2005, and IEEE Computer Society Outstanding Contribution Award in 2001 and 2009. Dr. Fujiwara is a life fellow of the IEEE, a Golden Core member of the IEEE Computer Society, a fellow of the IEICE and a fellow of the IPSJ.

"System Level Testing Considerations as we Move from RTL to ESL"

(Plenary Session 2; 9:00-10:10, Nov. 23, 2012)

Zainalabedin Navabi (University of Tehran)

Summary: In the last fifty years, design abstraction level has change from gate to RT-level, and now to ESL (Electronic System Level). In this path, new design and test methods evolve, and the older methods became too cumbersome and impractical for the complex new applications. Digital designers have already established RT level design methods, and based on that, well established test and testability methods have been put in place. Inspired from this, we will be looking at ESL that is a new abstraction level in digital systems, to find systematic methods of design and test. This talk focuses on ESL test methods. This level of abstraction uses IP- cores for its processing elements or components, and uses abstract channels for communicating between these components. We consider how RT level DFT methods translate to this new level of abstraction, and will look at test methods for testing communications at this level.

Biography: Dr. Zainalabedin Navabi is a professor of Electrical and Computer Engineering at the University of Tehran, and an adjunct professor at Worcester Polytechnic Institute. Dr. Navabi is the author of several textbooks and computer based trainings on VHDL, Verilog and related tools and environments. Dr. Navabi's involvement with hardware description languages begins in 1976, when he started the development of a register-transfer level simulator for one of the very first HDLs. In 1981 he completed the development of a synthesis tool that generated MOS layout from an RTL description. Since 1981, Dr. Navabi has been involved in the design, definition and implementation of Hardware Description Languages. He has written numerous papers on the application of HDLs in simulation, synthesis and test of digital systems. He started one of the first full HDL courses at Northeastern University in 1990. Since then he has conducted many short courses and tutorials on this subject in the United States, Europe and Asia. Since early 1990's he has been involved in developing, producing, and broadcasting online and video lectures on HDLs, Digital System Test, and various aspects of automated design. In addition to being a professor, he is also a consultant to CAE companies. Dr. Navabi received his M.S. and Ph.D. from the University of Arizona in 1978 and 1981, and his B.S. from the University of Texas at Austin in 1975. He is a senior member of IEEE, a member of IEEE Computer Society, member of ASEE, and ACM.