

SESSION 1: ATPG1

Chair: B. Courtois, INPG/TIMA, France

A Pragmatic Test Pattern Generation System for Scan-Designed Circuits with Logic Value Constraints.....

E.S. Park

An Optimal Scheme of Parallel Processing for Test Generation in a Distributed System.....

T. Inoue, T. Yonezawa, and H. Fujiwara

Proof that Akers' Algorithm for Locally Exhaustive Testing Gives Minimum Test Sets of Combinational Circuits with up to Four Outputs

H. Michinishi, T. Yokohira, and T. Okamoto

Universal Test Set Generation for CMOS Circuits

B. Chen and C.L. Lee

An Algorithm for Test Generation of Combinational Circuits — Research and Implementation for Critical Path Tracing.....

Y. Shi and D-Z. Wei

SESSION 2: Fault Tolerance

Chair: W.J. Hsu, Nanyang Technical University, Singapore

Reliable Fail-Safe Systems

M. Lubaszewski and B. Courtois

Study of Fault Propagation Using Fault Injection in the UNIX System

W-L. Kao, D. Tang, and R.K. Iyer

Neural Network Realization of Markov Model of TMR Systems with Compensating Failures.....

Y. Zhou and Y. Min

Software Upset Analysis: A Case Study of the HS1602 Microprocessor

G.S. Choi and R.K. Iyer

A Distributed Message Routing Algorithm for Fault-Tolerant Hypercube Systems

Y-L. Min and Y. Min

SESSION 3: Fault Simulation

Chair: F. Hirose, Fujitsu Lab. Ltd., Japan

A Two-Phase Fault Simulation Scheme for Sequential Circuits

W.C. Wu, C.L. Lee, and J.E. Chen

FASSAD: Fault Simulation with Sensitivities and Depth-First Propagation

P.R. Sureshkumar, J. Jacob, M.K. Srinivas, and V.D. Agrawal

On the Eliminating of Parameters α and β in STAFAN

J. Ding and J. Hu

Parallel Computation of LFSR Signatures.....

B. Narendran, M. Franklin, and K.K. Saluja

SESSION 4: Analog and Mixed Circuit Testing

Chair: C-S. Choy, Chinese University of Hong Kong

An Approach to the Analysis of the Current Testability of IC Analog Sections.....

D. Mateo, M. Roca, F. Serra-Graells, and A. Rubio

MISSED: An Environment for Mixed-Signal Microsystem Testing and Diagnosis

H.G. Kerkhoff and G. Docherty

Subjective Fault Evaluation Method of Electronic Circuits

M. Hashizume, Y. Iwata, and T. Tamesada

SESSION 5: ATPG2

Chair: M. Nakamichi, Chiba University, Japan

Test Generation for E-Beam Testing of VLSI Circuits

O.C.S. Choy, L.K. Chan, R. Chan, and C.F. Chan

PLANE: A New ATPG System for PLAs

J-D. Huang and W-Z. Shen

A 15-Valued Fast Test Generation for Combinational Circuits

S.J. Hong

Optimization of Deterministic Test Sets Using an Estimation of Product Quality

G. Spiegel and A.P. Stroele

SESSION 6: Software Testing

Chair: D. Tang, SoHaR Incorporated, USA

Testing of Parallel Programs Based on Primitive Dependence Graph

H-P. Wu

An Approach to Large Program Testing with Tool WHEN

H. Zhu and F. Chen

Test Sequence Algorithms and Formal Languages

S.P. Van de Burgt

A New Method for System Diagnosis

S. Xu and J. Gao

SESSION 7: BIST

Chair: L. Jin, Vertex Semiconductor, USA

A Global BIST Methodology

T. Gheewala, H. Sucar, and P. Varma

LFSROM: A Hardware Test Pattern Generator for Deterministic ISCAS85 Test Sets

C. Dufaza, C. Chevalier, and L.F.C.L.Y. Voon

Additive Cellular Automata as an On-Chip Test Pattern Generator

S. Nandi and P.P. Chaudhuri

T-BIST: A Built-In Self-Test for Analog Circuits Based on Parameter Translation

M. Slamani and B. Kaminska

SESSION 8: Fault Diagnosis

Chair: C-L. Lee, National Chiao Tung University, Taiwan

Test Set Partitioning and Dynamic Fault Dictionaries for Sequential Circuits

P.G. Ryan and W.K. Fuchs

Multiple Stuck-at Fault Diagnosis in Combinational Circuits Based on Restricted Single Sensitized Paths

H. Takahashi, N. Yanagida, and Y. Takamatsu

The Complexity of Determining the Sequential Diagnosability Number in the Malek's Comparison Model

L. Zhou, X. Yang, T. Chen, and C. Tang

Optimal Interconnect Diagnosis

W. Shi and W.K. Fuchs

Session 9: Panel — Testing Technology for Year 2000 Processor VLSIs

Organizer: K. Kinoshita, Osaka University Japan

Moderator: T. Yamada, Meiji University, Japan

Panelists:

T. Gheewala - CrossCheck, USA

K. Hatayama - Hitachi, Japan

F. Hirose - Fujitsu, Japan

M. Takada - NEC, Japan

Session 10: Panel — Effectiveness of BIST in Consumer Products

Organizer: Y. Zorian, AT&T Bell Laboratories, USA

Moderator: V.K. Agarwal, McGill University, Canada

Panelists: [to be announced]

Session 11: Design for Testability

Chair: M.W.T. Wong, Hong Kong Polytechnic

A C-Testable DCVS GF(2^m) Multiplier

T-Y. Chang, J-H. Chen, J-B. Hsu

The Driver/Receiver Conflict Problem in Interconnect Testing with Boundary-Scan

L. Jin

Design and Implementation of a JTAG Boundary-Scan Interface Controller.....

X-B. Shen and S-H. Liang

A Systematic Method to Classify Scan Cells.....

K-J. Lee, M-H. Lu, and J-F. Wang

GID-Testable Two-Dimensional Sequential Arrays for Self-Testing

W.K. Huang, F. Lombardi, and M. Lu

Session 12: IDDQ and Bridging Faults

Chair: Y-S. Tao, Information Technology Institute, Singapore

A Current Testing for CMOS Static RAMS to Reduce Testing Costs.....

H. Yokoyama, H. Tamamoto, and Y. Narita

Fault Modelisation of External Shorts in CMOS Circuits

M. Renovell, P. Huc, and Y. Bertrand

Limitations of Built-In Current Sensors (BICS) for I_{DDQ} Testing.....

S.M. Menon, Y.K. Malaiya, A.P. Jayasumana, and C.Q. Tong

Effectiveness of Stuck-at Test Sets to Detect Bridging Faults in Iddq Environment

S. Hwang and R. Rajsuman

Automatic Fault Location Using E-Beam and LSI Testers

N. Itazaki, T. Sumioka, S. Kajihara, and K. Kinoshita

Session 13: Testability Analysis

Chair: H. Hiraishi, Kyoto Sangyo University, Japan

Test Scheduling and Control in a Parallel Processing Environment.....

D. Xiang

On the Testability of Cascaded Reed Muller Circuits.....

G. Lee, M. Hwang, M.J. Irwin, and R.M. Owens

Detection of Multiple Faults Using SSFTS in CMOS Logic Circuits.....

C.Q. Tong and D. Lu

Session 14: Self-Checking

Chair: J-L. Chen, Beijing University of Post and Telecommunication, China

Design of Efficient Totally Self-Checking Checkers for m-Out-of-n Code

W-F. Chang and C-W. Wu

General Design Principles of Self-Testing Code-Disjoint PLAs	<i>S.J. Piestrak</i>
State Encoding and Functional Decomposition for Self-Checking Sequential Circuit Design.....	<i>S. Pagey, S.D. Sherlekar, and G. Venkatesh</i>
Design of Monitored Self-Checking Sequential Circuits for Enhanced Fault Models	<i>R.A. Parekhji, G. Venkatesh, and S.D. Sherlekar</i>
Session 15: Signature Analysis	
<i>Chair: E. Wu, AT&T Engineering Research Center, USA</i>	
On Properties and Implementations of Inverting ALSC for Use in Built-In Self-Testing	<i>K. Furuya, P.Y. Koh, and E.J. McCluskey</i>
Achieving Minimal Hardware Multiple Signature Analysis for BIST.....	<i>Y. Wu and A. Ivanov</i>
Error Localization in Test Outputs: A Generalized Analysis of Signature Compression	<i>S. Demidenko, V. Piuri, and A. Ivaniukovich</i>
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<i>Chair: S.D. Sherlekar, Indian Institute of Technology, India</i>	
Application of Homing Sequences to Synchronous Sequential Circuit Testing.....	<i>I. Pomeranz and S.M. Reddy</i>
Computer Aided Testing System of LC Cell's Optical Properties	<i>M. Jiang, X. Huang, Z. Wang, and Z. Lin</i>
Bayesian Inference for Fault Diagnosis in Real-Time Distributed Systems	<i>Y.L.C. Chang, L.C. Lander, H-S. Lu, and M.T. Wells</i>
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<i>Chair: D-Z. Wei, ICT, Academia Sinica, China</i>	
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P.2 — An Effective Off-Line Fault Diagnosis Method for PCB in SPC Digital Switching System-Functional Module Oriented Test Technique	<i>L. Li and X. Xu</i>
P.3 — The Application of Reverse Time Processing in FD-II ATPG System	<i>W. Huang, X. Chen, L. Zhao, and B. Liu</i>
P.4 — TeDS-A Test Development System — An Outline of TeDS	<i>Q.L. Yang</i>
P.5 — Integrating Built-In Self-Test into a PC System Controller Chip	<i>M.W.T. Wong and W.M. Lo</i>
P.6 — A Serial Feedback Built-In Self-Test Scheme	<i>X. Li and F. Tsui</i>
P.7 — Intelligent Off-Line Test Program Debugging for VLSI Test Systems	<i>Y. Ma and W. Shi</i>
P.8 — A Tool to Generate Test Cases from SDL Specifications	<i>T. Su, J.L. Chen, and S.D. Cheng</i>
P.9 — The Test Pattern Generation of a Universal Logic Tester	<i>J. Huang, T. Xiao, and Z. Chen</i>
P.10 — A Methodology of Fault Injection	<i>Z. Wu and X. Yang</i>